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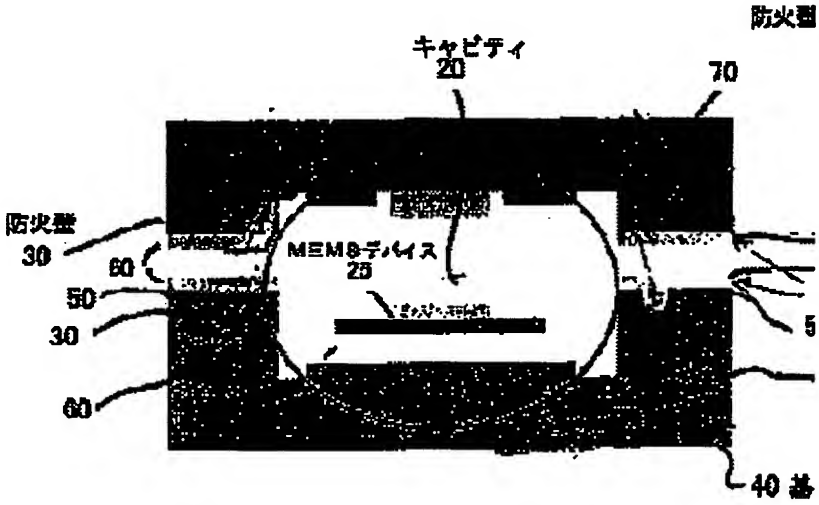
(54) PACKAGE HAVING CAVITY FOR HOUSING MEMS

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a package technology for sealing an MEMS device hermetically so that the MEMS device can be built in a CMOS circuit.

SOLUTION: The inventive package technology can be employed for packaging an MEMS device according to a conventional CMOS package technology. The invention also provides means for controlling the operational environment of the MEMS device. In the inventive package, a protected cavity is provided around an MEMS device fabricated by a flip-chip bonding process. According to one embodiment, a firewall is formed on a first substrate around the MEMS device which is sealed in a cavity bounded by the firewall. Subsequently, another substrate is flip-chip bonded to the first substrate holding the MEMS device.



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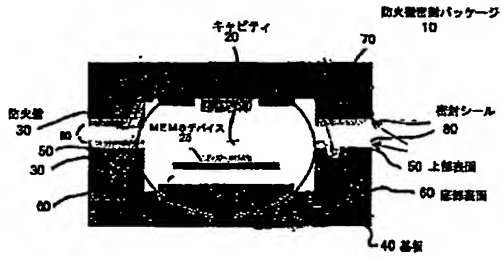
最終頁に続く

(54)【発明の名称】　ＭＥＭＳデバイスを有能するキャビティを具備するパッケージ

(57)【要約】
【課題】　ＭＥＭＳデバイスがＣＭＯＳ回路等組み込むことができるように、ＭＥＭＳデバイスを気密にシールするパッケージ技術を提供すること。
【解決手段】本発明のパッケージ技術は、従来のＣＭＯＳパッケージ手順がＭＥＭＳデバイスをパッケージするのに用いることができるようにする。さらに本発明は、同時にＭＥＭＳデバイスの動作環境を制御する手段を提供する。本発明のパッケージは、フリップチップ接合プロセスにより形成されたＭＥＭＳデバイスの周囲に、保護されたキャビティを提供する。本発明の一実施例によれば、防火壁がＭＥＭＳデバイスの周囲の第１基板上に形成され、防火壁により結合されたキャビティ内にＭＥＭＳデバイスを封止する。その後別の基板が、ＭＥＭＳデバイスを保持している第１基板に、フリップチップ結合される。



【特許請求の範囲】
【請求項１】　マイクロ電子機械システム（ＭＥＭＳ）デバイスを収納し、このＭＥＭＳデバイスをキャビティ内にシールして、パッケージがさらされる劣悪環境に対しＭＥＭＳデバイスを保護する高さを具備するキャビティを有するパッケージにおいて、
ＭＥＭＳデバイスがその上に形成されるベースを規定する第１基板と、
前記第１基板上に形成され、前記第１基板の係合する底部表面を有する防火壁と、からなり、
前記防火壁は、底部表面から上方にのびるキャビティの壁を形成して、前記防火壁と第１基板とにより形成され、結合されるキャビティ内に、前記ＭＥＭＳデバイスを完全に収納し、
前記防火壁の上で、前記第１基板に結合され、前記防火壁と契合してシールして、パッケージが配置される劣悪環境に対し、ＭＥＭＳデバイスを完全に収納するようキャビティを包囲するシールを形成する第２基板と、からなり、
前記ＭＥＭＳデバイスは、キャビティ内に収納されて、劣悪環境から保護されることを特徴とするキャビティを具備するパッケージ。
【請求項２】　前記２枚の基板から離間して、前記２枚の基板の一方または両方のいずれかの上に形成され、前記キャビティの高さを規定する複数のスペーサをさらに有し、
前記第２基板は、複数のスペーサとシールしながら係合して、前記キャビティの上に配置されることを特徴とする請求項１記載のパッケージ。
【請求項３】　前記シールは気密シールであることを特徴とする請求項１記載のパッケージ。
【請求項４】　前記気密シールは、前記防火壁の上部表面の少なくとも一部を覆うような金属製のフィルムを含むことを特徴とする請求項３記載のパッケージ。
【請求項５】　前記気密シールは、前記防火壁の上部表面にはんだ付けされた金属製のフィルムを含み、前記気密シールがパッケージに対し機械的強度および構造的な一体性を与えることを特徴とする請求項４記載のパッケージ。
【請求項６】　前記気密シールによる機械的強度を補助するために、前記パッケージに機械的一体性を与える、第１基板上に形成された複数のはんだバンプをさらに有することを特徴とする請求項５記載のパッケージ。
【請求項７】　前記金属製フィルムは、金製であることを特徴とする請求項６記載のパッケージ。
【請求項８】　前記金属製フィルムは、銀製であることを特徴とする請求項６記載のパッケージ。
【請求項９】　前記金属製フィルムは、金の合金製であることを特徴とする請求項６記載のパッケージ。
【請求項１０】　前記金属製フィルムは、銀の合金製であることを特徴とする請求項６記載のパッケージ。
【請求項１１】　前記防火壁は、ポリシリコンにより包囲された、ポリシリコンと二酸化シリコンを交互に重ねた積層構造を含むことを特徴とする請求項１記載のパッケージ。
【請求項１２】　前記キャビティ内のＭＥＭＳデバイスに接続され、前記防火壁を貫通してのびるリード線をさらに有することを特徴とする請求項１記載のパッケージ。
【請求項１３】　前記リード線は、二酸化シリコン層により包囲され、さらに別のポリシリコン層により包囲されたポリシリコン層を含むことを特徴とする請求項１２記載のパッケージ。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、マイクロ電子機械システム（micro-electromechanical systems：ＭＥＭＳ）デバイスのパッケージに関し、特に、ＭＥＭＳデバイスに気密シールを与えるフリップチップ接合方式のＭＥＭＳデバイスのパッケージに関する。
【０００２】
【従来の技術】ＭＥＭＳデバイスは、半導体業界では至るところに見られ、多くの電子システムおよび電子光学システムに必要とされる合成電子機能部品、および機械部品で用いられる。このようなシステムでＭＥＭＳデバイスをパッケージすることは、通常コストのかかるプロセスである。機械的部分は、ＭＥＭＳ機能部品の主要な部分であるために、動作用の注意深く設計されたスペースが、ＭＥＭＳデバイスが信頼性高く動作するためには必要である。ＣＭＯＳ電子部品に用いられる従来のパッケージ技術は、ＣＭＯＳデバイスがパッシベーション材料により適宜保護された後実行される。このようなパッシベーション手順は、通常機械的および化学的に厳しい状態を作り出すパッケージプロセスからデバイスを保護するものである。デバイスのパッシベーション後、パッケージは、溶融プラスティック材料、あるいはエポキシ材料を、ＣＭＯＳチップを覆うように注入することにより行われる。ＣＭＯＳの機能は、シリコンの電子的特性に依存するために、このようなパッケージプロセスは、デバイスの性能を劣化させてはならない。しかしこのようなパッケージ技術は、流体を用いて半導体チップを処理することになり、そのため、ＭＥＭＳデバイスの動作と適合性を有さない。このため、ＭＥＭＳデバイスに対しては高価なセラミックパッケージ技術が安いプラスティックモールドパッケージに代わって選択されている。
【０００３】多くのＭＥＭＳデバイスは、最適なデバイス性能および信頼性を確保するために、制御された環境のもとで動作する必要がある。このような制御された環境の例は、圧力を制御すること（真空にすること）、湿度を制御すること、および化学環境（特殊ガス）を制御

することである。このような条件のもとで、効果的にMEMSデバイスをパッケージすることが必要であるが、MEMSデバイスの動作環境の複雑さおよび感受性の高さに起因してそれは困難および実現が難しい。

【0004】このような効果的なMEMSパッケージ技術を、CMOSパッケージ技術と適合性を持たせることが必要である。これはCMOS技術がすでに確立し、市場で用いられているために重要である。さらにまたCMOS技術でMEMSデバイスを集積化する必要性は、単一のCMOSデバイスが与えることのできないCMOSチップに機能を追加するため、およびCMOS集積回路を用いてMEMSデバイスの制御を与えるためにますます重要となる。しかしウェット化学処理、および高圧流体流が用いられるような多くのCMOSパッケージ技術は、MEMSデバイスに損傷を与える。かくして、現在のCMOSパッケージ技術は、パッケージプロセス内でMEMSデバイスを十分の保護することができない。

【0005】

【発明が解決しようとする課題】本発明の目的は、MEMSデバイスがCMOS回路、および他の混成回路で組み込むことができるように、MEMSデバイスを気密にシールするパッケージ技術を提供することである。本発明のパッケージは、安価でかつパッケージの完全性を破ることなくMEMSデバイスとの電気的接続が確保できる。さらにまた本発明のパッケージは、現在の半導体製造プロセスと容易に一体化でき、従来のCMOSパッケージ方法と適合性を有するものである。

【0006】

【課題を解決するための手段】本発明のパッケージ技術は、従来のCMOSパッケージ手順がMEMSデバイスをパッケージするのに用いることができるようにする。さらに本発明は、同時にMEMSデバイスの動作環境を制御する手段を提供する。本発明のパッケージは、フリップチップ接合プロセスにより形成されたMEMSデバイスの周囲に、保護されたキャビティを提供する。本発明の一実施例によれば、防火壁がMEMSデバイスの周囲の第1基板上に形成され、防火壁により結合されたキャビティ内にMEMSデバイスを封止する。その後別の基板が、MEMSデバイスを保持している第1基板に、フリップチップ結合される。

【0007】この第2基板が、他のMEMSデバイスを保持して、混成回路の構造および機能を完成させ、またCMOS電子部品を保持して第1基板および／または第2基板上のMEMSデバイスを制御し、あるいはMEMSデバイスの防火壁の機械的カバーとして機能する。2枚の基板の間のギャップは、防火壁そのものの高さにより、あるいは公知の高さのスペーサにより、あるいは防火壁とスペーサの組合せにより正確に制御される。スペーサは、基板上に独立に形成されるが、この場合スペーサは、そのままでは防火壁の一部を構成しない。本発明の一実施例においては、キャビティは密封され、すなわちキャビティはパッケージの周囲に対しシールされ、MEMSデバイスをパッケージの使用環境の悪条件から保護する。

【0008】2枚の基板をフリップチップ結合した後、防火壁がMEMSデバイスの周りのスペースを封止する。同時に機械的なサポートと一体性が適宜の接合技術により接合された基板によりパッケージに与えられる。さらに本発明の別の実施例においては、密封防火壁そのものがパッケージの機械的サポートを与える。さらに好ましくは、独立構造をパッケージに与えて、パッケージにさらに機械的にサポートを与える。キャビティが防火壁により形成され、MEMSデバイスがそれに応じて保護されると、MEMSデバイスをパッケージ内に保持する混成チップが、従来のCMOSパッケージ技術を用いてさらにパッケージ（封止）される。

【0009】本発明のMEMSデバイスのパッケージは、その実現が容易で、かつ従来のCMOSパッケージ技術とともに容易に実行できる。さらにまた本発明のパッケージは、MEMSデバイスに損傷を与えるようなパッケージに悪使用環境からMEMSデバイスを気密にシールして保護する。かくして本発明のパッケージは、MEMSデバイスを保護し、これらのデバイスが有効に機能する。

【0010】

【発明の実施の形態】図1に本発明の防火壁密封パッケージ10を示す。防火壁密封パッケージ10は、MEMSデバイスが集積される混成回路のアプリケーションに応じて、1つ、あるいは複数のMEMSデバイス25を収納するキャビティ20を有する。本発明の一実施例においては防火壁30は、MEMSデバイスが形成される基板40と基板70の一方、あるいは両方の上に形成される。防火壁30は上部表面50と底部表面60を有する。防火壁密封パッケージ10は基板70を有し、この基板70は、基板40に形成された防火壁30を介して第1の基板40に結合される。第2の基板70は、防火壁30に適合するシールを有し、これにより防火壁構造体を完成させる。好ましくは第2の基板70は、基板40に、適宜の結合技術を用いてフリップチップ結合される。好ましい結合技術は、加熱プロセスであり、金属あるいはプラスティックレジンのような材料を接合されるべき2つの部品の間に配置して、加熱して溶融、あるいは材料を溶融、あるいは軟化させるものである。その後材料が固くなると、強くかつ柔軟なシールが2つの部品の間に形成される。

【0011】基板40、70は、CMOS電子デバイスを形成するのに用いられる従来の基板である。このような基板はシリコン製であるが、他の材料、例えばGaAs、Ge、あるいは他の半導体材料、あるいは水晶、アルミナ、サファイアのような絶縁材料で基板を形成して

もよい。以下の説明においては基板は、シリコン製基板とする。ただしこれに限定されるものではない。

【0012】防火壁30はMEMSデバイス25の周囲に形成されるが、基板40、70の一方に形成してもよい。防火壁30の高さを精密に制御して、2枚の基板の間のスペースを制御する。ある種のMEMSデバイスにおいては、このスペースは、MEMSデバイスの一体化された一部であるが、他のデバイスにおいてはキャビティ20内にMEMSデバイスを収納するのに十分な大きさでもよい。シール材料を防火壁30の上部に採用して、キャビティ20に対する密封シール80を生成する。シール材料は薄い金属製フィルム材料で、防火壁30の上部表面50の少なくとも一部の上に配置して、基板70を基板40にフリップチップ結合したときにキャビティ20をシールする。フリップチップ結合プロセスの間、基板の両面上の接合（溶接）材料を加熱して圧縮して、フリップチップ結合された基板40、70の間に気密シールを形成する。フリップチップ結合プロセスの後、防火壁30により形成されたキャビティ20と、基板40、70が、MEMSデバイス25の周囲の小さなスペースを包囲する。これによりMEMSデバイス25は他には接触せず、MEMSデバイス25に対し悪影響を及ぼすような流体処理を含む、キャビティ20の外部で行われる後続のパッケージプロセスから保護する。

【0013】本発明の気密防火壁は、MEMSデバイスを製造するのに用いられる同一のプロセスを用いて形成することができる。シリコン表面の微細加工技術を用いて形成されたMEMSデバイスの例においては防火壁は、多結晶シリコンと二酸化シリコンを交互に積層して、多結晶シリコンで包囲することにより形成される。別の方法は、リソグラフ技術を用いて基板上で堆積、あるいはスピンコートし、パターン化された材料を用いる。ある種の実施例では、窒化シリコン、ポリイミド、金属を用いる。これらすべての場合、防火壁30を有する材料は、所望の化学的および機械的強度を有し、基板と防火壁との間に気密シールを形成してMEMSデバイス25を保護する。このような技術を用いて、防火壁の高さを正確に形成できる。

【0014】図2に示した実施例においては、第1基板と第2基板上の防火壁間の密封シール80は、金、銀、あるいはそれらの合金のような軟金属を、防火壁30の上部表面に蒸着し、金属表面を加熱しながら圧着することにより形成される。この加熱は、第1基板を第2基板にフリップチップ結合するプロセスの間行われるか、あるいは独立に加熱するプロセス、あるいははんだ付けするプロセスにより行われる。しかし、密封シール80を形成することは、基板を一体に保持し、防火壁密封パッケージ10に対する機械的な完全性を耐えるには十分な機械的強度を与えることはない。より強い機械的なシールは、従来のフリップチップ結合パッケージ技術で用いられる、より強いはんだ技術を用いて達成される。より強い機械的な支持を与えるために、さらにはんだを用いることが望ましい場合には、複数のはんだバンプ90を基板40に結合して、第2の基板（図2に図示せず）を第1基板にフリップチップ結合するときに、パッケージに対し機械的な支持および一体性を与える。別の方法としてはんだバンプ90を第2基板に結合するが、これは単なる設計的事項である。

【0015】本発明によりMEMSデバイスのパッケージの製造に際し重要な点は、MEMSデバイス25と残りの回路との電気的接続は、MEMSデバイス25を破らずに防火壁30を横切らなければならない点である。本発明の一実施例においては、MEMSデバイス25を残りの回路に接続するリード線100は、MEMS製造プロセスの間防火壁30を貫通して挿入される。この場合、例えばリード線は、濃くドープした導電性の多結晶シリコンで形成し、二酸化シリコン層で包囲して電気的絶縁を確立する。本発明の他の実施例においては、リード線100は防火壁30の下に配置することもできる。別の構成としてリード線100をCMOS回路を含む第2の基板70に固定し、リード線100がそこを横切ることにより防火壁30を破損することがないようにする。この場合基板40上のMEMSデバイス25と、基板70上のリード線との間の電気的接続が形成されねばならない。このような接続は、はんだバンプ手段、あるいは独立したスペーサ120を金属化処理することにより容易に達成できる（図3）。

【0016】図2の実施例においては、防火壁30は、多結晶シリコン層とに酸化シリコン層の積層体を含む。防火壁30そのものは、防火壁30の高さがキャビティ20の高さを規定するように、基板40と基板70の間のギャップを制御するために、キャビティ20に対するスペーサとして機能する。機械的な強度は、防火壁30の外側に配置されたはんだバンプ90により与えられる。このはんだバンプ90は、基板40、70の一方、あるいは両方の上の適宜の場所に配置することができる。リード線100は、二酸化シリコン層により包囲され、さらに別のポリシリコン層により封止されたポリシリコンを有する。

【0017】図3は防火壁30を有する本発明のリード線100の他の実施例を示す。上記のごとく、金属製フィルムを防火壁30の構造体の上部表面50の上に蒸着して、キャビティ20に対する密封シール80を形成する。はんだ材料を、防火壁30の上部表面50の上に堆積して、キャビティ20に対するはんだシール110を生成する。はんだシール110が形成されるとそれは、強固な密閉パッケージを生成するフリップチップ接合プロセスに必要な機密性と機械的強度の両方を与える。独立したスペーサ120は、基板間に必要とされるギャップ、すなわちスペースを正確に規定するために具備され

る。スペーサ１２０は基板４０、７０の一方、あるいは両方の任意の場所に配置することができる。

【００１８】はんだバンプ、あるいはリング形状のはんだシールのプロセスを、図４ａ－ｃに示す。はんだバンプ、あるいはリング形状のはんだシール接合を用いた実施例においては、スペーサ１２０の高さは、はんだバンプよりも意図的に高くしてある。はんだバンプを用意するために、はんだ７５を、はんだが濡れない８５の上で金属パッドよりもより広い面積に堆積する（図４ａ）。加熱すると、表面張力によりはんだバンプ９０が高くなって、その底面積を減少させる（図４ｂ）。このメカニズムによりはんだバンプ９０は、他の基板上の金属パッド９５に接触するようになる。冷却するとはんだは縮んで、２の基板を引きつける（図４ｃ）。このプロセスによりスペーサの間の正確な接続、および２枚の基板の間の正確な分離が可能となる。

【００１９】図３の実施例の欠点は、フラックス材料（気層、または液層のいずれか）がはんだに必要な場合には、ＭＥＭＳデバイス２５はこの環境にさらさせる点である。これは適切なフラックスが使用される場合には、ＭＥＭＳデバイス２５に悪影響を及ぼさないが、ＭＥＭＳデバイス２５に対し制御した環境を与える機能を制限する。

【００２０】図５は、本発明の気密防火壁を含むはんだシール１１０の他の実施例を示す。この実施例においては、二重の防火壁構造が基板４０と基板７０の上に形成される。内側壁１３０は図１のそれと同様であり、金属層８０が防火壁３０の上部表面５０の上に堆積され、キャビティ２０に対する適切なスペースを与える。外側壁１４０は図３の防火壁３０と同様であり、はんだシール１１０が防火壁３０の上部表面５０の上に堆積される。その結果得られたパッケージの機械的強度は、外側壁１４０により与えられる。この実施例においては内側壁１３０は、基板４０、７０に２つの金属層８０の間のタック結合により結合される。このタック結合は、はんだ材料層１１０のはんだの溶融温度に比較してそれよりも低い温度で、２枚の基板の間に圧力を加えることにより得られる。このプロセスは制御した環境下で行われ、内側壁１３０により封止されたスペースがこの環境を維持し、そして封じきられる。低温のタック結合が行われた後、基板４０、または基板７０をはんだを溶かすのに十分な温度まで加熱して、外側壁１４０の上にはんだ接合を形成する。図４の二重の防火壁は、ＭＥＭＳデバイス２５をはんだプロセスの悪影響から保護できる利点がある。なお、金属層８０と密封シール８０は同一の機能を有するものである。また、はんだシール１１０とはんだ材料層１１０も実質的に同一である。

【００２１】防火壁により形成されたキャビティ内の環境は、所望の環境下でフリップチップ接合プロセスを実行することにより制御できる。このような所望の環境は、圧力を制御すること、湿度を制御すること、およびガスの性質を制御することが含まれる。フリップチップ接合プロセスにより形成されたキャビティ２０が、ＭＥＭＳデバイスを保護し、その結果フリップチップ結合された基板は、ＭＥＭＳデバイスに対し悪影響を及ぼすことのある従来のパッケージ技術を用いてパッケージ（封止）することができる。

【図面の簡単な説明】

【図１】本発明によるＭＥＭＳデバイスを封止する防火壁密封デバイスの断面図。

【図２】防火壁がスペーサとして機能し、防火壁の外側にあるはんだバンプにより機械的サポートが与えられる防火壁密封パッケージの斜視図。

【図３】防火壁が機械的サポートを与えるリング形状はんだシールドを有し、スペーサが具備される本発明の防火壁密封パッケージの斜視図。

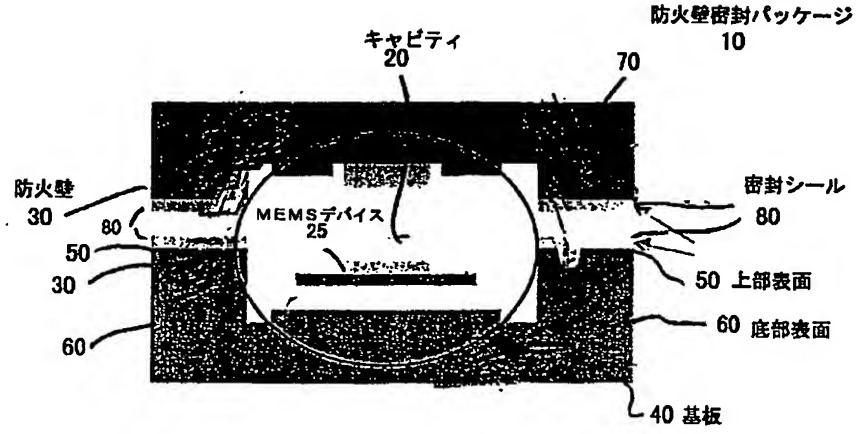
【図４】ａ－ｃは、はんだバンプ、あるいはリング形状のはんだシールを形成するプロセスを表す図。

【図５】ＭＥＭＳシールを行う内側壁と、パッケージに第２の密封シールと、機械的サポートを与えるリング形状のはんだシールを有する外側壁からなる、二重壁構造の本発明の防火壁密封パッケージの斜視図。

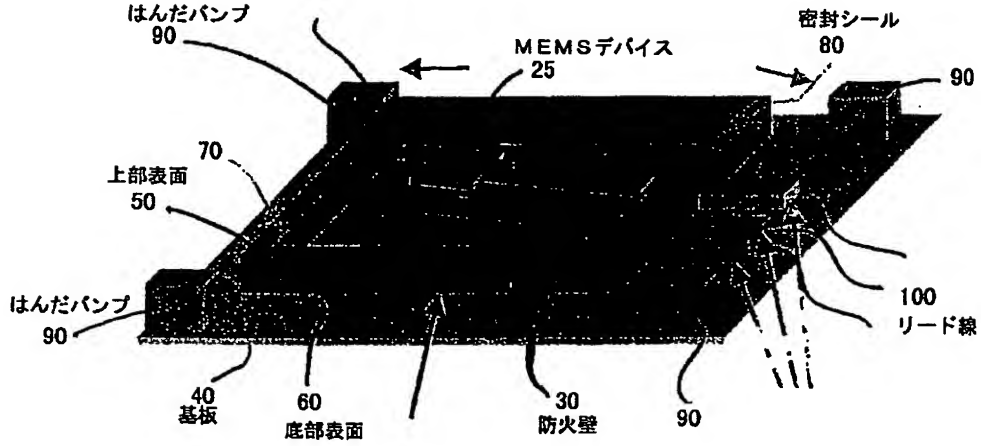
【符号の説明】

１０　防火壁密封パッケージ
２０　キャビティ
２５　ＭＥＭＳデバイス
３０　防火壁
４０、７０　基板
５０　上部表面
６０　底部表面
８０　密封シール（図１、２）
８０　金属層（図５）
９０　はんだバンプ
９５　金属パッド
１００　リード線
１１０　はんだシール（図３）
１１０　はんだ材料層（図５）
１２０　スペーサ
１３０　内側壁
１４０　外側壁

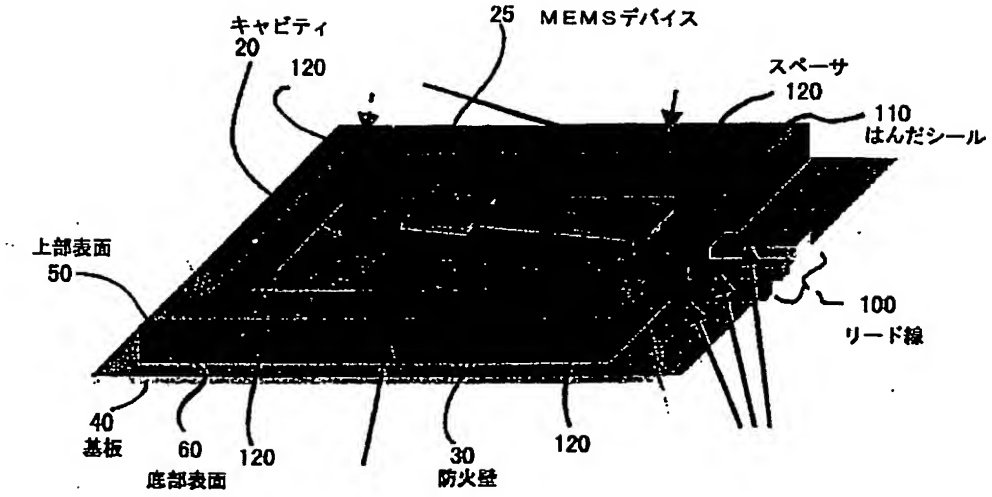
【図1】


防火壁密封パッケージ
10
キャビティ
20
70
防火壁
30
80
50
30
60
MEMSデバイス
25
密封シール
80
50 上部表面
60 底部表面
40 基板

【図2】

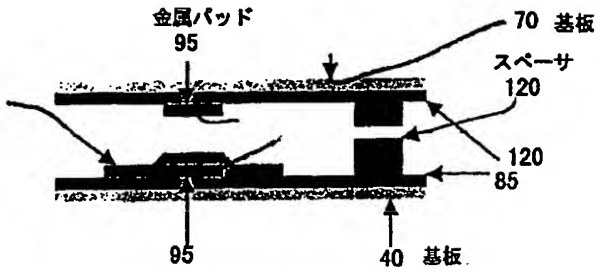

はんだバンプ
90
MEMSデバイス
25
密封シール
80
90
70
上部表面
50
はんだバンプ
90
100
リード線
40
基板
60
底部表面
30
防火壁
90

【図3】

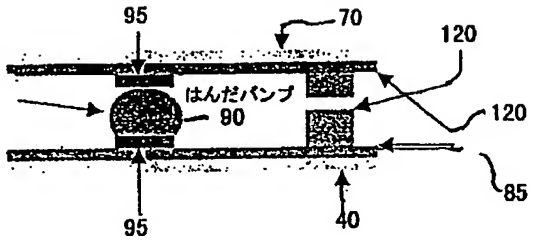

キャビティ
20
120
25 MEMSデバイス
スペーサ
120
110
はんだシール
上部表面
50
100
リード線
40
基板
60
底部表面
120
30
防火壁
120

【図4】

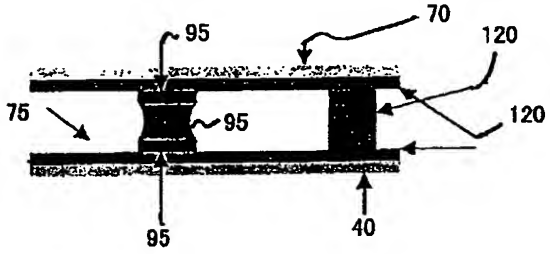
a


金属パッド
95
70 基板
スペーサ
120
120
85
95
40 基板

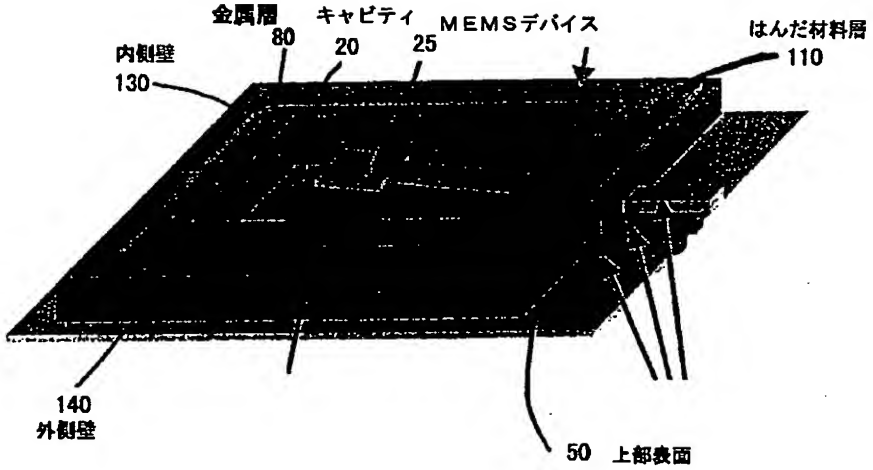
b


95
70
120
はんだバンプ
90
120
85
95
40

c


95
70
120
75
95
120
95
40

【図5】


金属層
80
キャビティ
20
25
MEMSデバイス
はんだ材料層
110
内側壁
130
140
外側壁
50 上部表面

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【外国語明細書】

1. Title of Invention

Hermatic Firewall For MEMS Packaging In Flip-Chip Bonded Geometry

2. Claims

1. A package having a cavity with a height for housing a micro-electromechanical systems (MEMS) device and sealing the MEMS device in the cavity to protect the MEMS device against deleterious conditions present in an environment of the package, comprising:

a first substrate for defining a base on which the MEMS device is fabricated;

a firewall fabricated on the first substrate and having a bottom surface engaged with the first substrate, said firewall forming walls of the cavity which extend upwardly away from the bottom surface, for fully surrounding the MEMS device within the cavity which is bounded and formed by the firewall and the first substrate; and

a second substrate bonded to the first substrate over the firewall and in sealed engagement with the firewall for creating a cavity-closing seal for the cavity within which the MEMS device is fully enclosed against the deleterious conditions present in the environment of the package so that the MEMS device is be packaged protectedly within the cavity and remote from the deleterious conditions.

2. The package of claim 1, further comprising a plurality of spacers formed on either one or both of the two substrates to predeterminedly space apart the two substrates and thereby define a height of the cavity, and wherein the second substrate is placed over the cavity in further sealed engagement with the plurality of spacers.

3. The package of claim 1, wherein the seal is a hermetic seal.

4. The package of claim 3, wherein the hermetic seal comprises a thin film metal material overlaying at least a portion of a top surface of the firewall.

5. The package of claim 4, wherein the hermetic seal comprises a thin film metal material soldered to the top surface of the firewall to produce the hermetic seal having a mechanical strength and imparting structural integrity to the package.

6. The package of claim 5, further comprising a plurality of solder bumps fabricated on the first substrate for providing mechanical integrity to the package to supplement the mechanical strength provided by the hermetic seal and thereby assure sufficient mechanical integrity for the package.

7. The package of claim 6, wherein the thin film metal material comprises gold.

8. The package of claim 6, wherein the thin film metal material comprises silver.

9. The package of claim 6, wherein the thin film metal material comprises an alloy of gold.

10. The package of claim 6, wherein the thin film metal material comprises an alloy of silver.

11. The package of claim 1, wherein the firewall comprises alternating stacks of poly-silicon and silicon dioxide encapsulated by poly-silicon.

12. The package of claim 1, further comprising electrical leads connected to the MEMS device in the cavity and extending through the firewall.

13. The package of claim 12, wherein the electrical leads comprise a poly-silicon layer surrounded by a silicon dioxide layer which is further surrounded by another layer of poly-silicon.

3. Detailed Description of Invention

Field of the Invention

The present invention relates to packaging for micro-electromechanical systems (MEMS) devices. More specifically, the present invention relates to packaging of MEMS devices in flip-chip bonded geometry to provide hermetic seals for the MEMS devices.

Description of the Related Art

MEMS devices have become ubiquitous in the semiconductor industry and are used in hybrid electrical and mechanical functions that are necessary in many electronic and electro-optical systems. Packaging MEMS devices in such systems is in general a costly process. Because mechanical motion is an essential part of the MEMS function, a carefully designed space for the motion is needed in order for the MEMS device to operate reliably. Conventional packaging techniques used for CMOS electronics are performed after the CMOS devices are appropriately protected using proper passivation material. Such passivation procedure protects the devices from the packaging processes that are usually mechanically and chemically harsh. After device passivation, packaging is performed by injecting either molten plastic or epoxy over the CMOS chip. Since the CMOS function relies purely on the electronic properties of silicon, such a packaging process does not interfere with device performance. However, these packaging techniques usually involve treatment of semiconductor chips using a fluid, and are therefore not compatible with MEMS device operation. For this reason, expensive ceramic packaging has usually been chosen over cost-effective plastic molded packages for MEMS devices.

Most MEMS devices need to operate in a controlled environment to achieve optimum device performance and reliability. Some examples of controlled environments include controlled pressure (vacuum), controlled humidity, and

controlled chemical (typically a special gas) environments. Packaging MEMS devices cost-effectively under these conditions is desired in the art, but due to the complexities and sensitivities associated with operation environments of MEMS devices it is often a difficult or impractical task.

It is also essential that such cost-effective MEMS packaging technology be compatible with CMOS packaging technology. This is important because CMOS technology is already mature and commercially available. Moreover, the need to integrate MEMS devices with CMOS technology is becoming increasingly important in order to add functionality to the CMOS chip that simple CMOS devices cannot provide, and to provide control of MEMS devices using CMOS integrated circuits. Most CMOS packaging techniques wherein wet chemistry and high-pressure fluid flows are used, however, are detrimental to MEMS devices. Thus, current CMOS packaging techniques will not adequately protect the MEMS devices during the packaging process.

Accordingly, there is a long-felt, but unresolved need in the art for MEMS packaging techniques which hermetically seal the MEMS devices so that they can effectively be incorporated in CMOS and other hybrid circuits. The packages should be cost-effective and ensure that electrical connections to or with the MEMS devices can be achieved without breaching the integrity of the package. Moreover, such packages should be easily integratable with current semiconductor fabrication processes and be compatible with conventional CMOS packaging methods.

Summary Of The Invention

The present invention provides a novel packaging technique that enables conventional CMOS packaging procedures be used to package MEMS devices. It also provides means to control the operation environment of the MEMS devices at the same time. The inventive packages produce a protected cavity around the MEMS devices which is created by a a flip-chip bonding process. In a preferred embodiment, a firewall is fabricated on a first substrate around the MEMS device to

enclose the MEMS device within the cavity bounded by the firewall. Another substrate is then flip-chip bonded to the first substrate that holds the MEMS device. This second substrate may hold other MEMS devices to complete the structure or functionality of the overall hybrid circuit, may hold CMOS electronics to control the MEMS device(s) on the first and/or second substrate, or may serve purely as a mechanical "cover" of the MEMS device firewall. A gap between the two substrates is accurately controlled by the height of the firewall itself, by spacers of known height, or with spacers in conjunction with the height of the firewall. The spacers can be fabricated independently on the substrate, in which case they will not form a portion of the firewall *per se*. In a preferred embodiment, the cavity is hermetic, which means that the cavity is sealed against the environment of the package to protect the MEMS device from any deleterious conditions found or present in the environment of the package.

Upon flip-chip bonding of the two substrates, the firewall seals off the space immediately around the MEMS device(s). At the same time, mechanical support and integrity is provided for the package by the bonded substrates through appropriate bonding techniques. In still a further preferred embodiment, the hermetic firewall itself provides the mechanical support for the package. Still more preferably, independent structures are provided to the package to give the package its additional mechanical support. Once the cavity has been created by the firewall and the MEMS device is protected accordingly, the hybrid chip containing the MEMS device in its package can be further packaged using conventional CMOS packaging technology.

The inventive packages for MEMS devices are simple to implement and can easily be performed with conventional CMOS packaging technology. Moreover, packages provided in accordance with the present invention may hermetically seal MEMS devices from deleterious effects found in a packaging environment which could damage the MEMS devices. Thus, the packages disclosed and claimed herein efficiently protect MEMS devices so that these devices can function robustly when in use.

These and other features of the present invention will become apparent from the following detailed description considered in conjunction with the accompanying drawings. It is to be understood, however, that the drawings are designed solely for purposes of illustration and not as a definition of the limits of the invention, for which reference should be made to the appended claims.

Other objects and features of the present invention will become apparent from the following detailed description considered in conjunction with the accompanying drawings. It is to be understood, however, that the drawings are designed solely for purposes of illustration and not as a definition of the limits of the invention, for which reference should be made to the appended claims. It should be further understood that the drawings are not necessarily drawn to scale and that, unless otherwise indicated, they are merely intended to conceptually illustrate the structures and procedures described herein.

Brief Description Of The Drawings

In the drawings, wherein like reference numerals identify similar elements throughout the several views:

Figure 1 is a schematic, cross-sectional view of a hermetic firewall package for enclosing MEMS devices in accordance with the present invention;

Figure 2 is an elevated perspective view of a hermetic firewall MEMS package wherein the firewall serves as a spacer while mechanical support is provided by solder bumps outside of the firewall;

Figure 3 is a perspective view of a hermetic firewall MEMS package of the invention wherein the firewall includes a ring-shaped solder seal that provides the mechanical support and spacers are provided separately;

Figures 4a-c depict a schematic process of solder bump or ring-shaped solder seal; and

Figure 5 is an elevated perspective view of a hermetic firewall MEMS package of the invention wherein a double-walled structure is implemented and wherein an inner wall provides the MEMS sealed environment while an outer wall includes a ring-shaped solder seal that provides a second hermetic seal and mechanical support for the package.

Detailed Description Of The Presently Preferred Embodiments

Referring now to the drawings, Figure 1 depicts a schematic cross-sectional view of the hermetic firewall structure of the present invention identified by the general reference numeral 10. The package 10 comprises a cavity 20 for enclosing a MEMS device 25 or several MEMS devices, depending on the particular hybrid circuit application in which the MEMS device(s) will be integrated. In a preferred embodiment, a firewall 30 is fabricated on one or both substrates 40 and 70 on one of which the MEMS device is fabricated. The firewall 30 includes a top surface 50 and a bottom surface 60. The package 10 further comprises a second substrate 70 which is bonded to the first substrate through the firewall 30 formed on substrate 40. The second substrate 70 contains a mating seal to the firewall 30, which completes the firewall structure. Preferably, the second substrate is "flip-chip" bonded to substrate 40, using a suitable bonding technique. A preferred bonding technique is a heat-based process wherein a material such as a metal or plastic resin is placed between two parts to be welded together and heated to melt or soften the material. When the material thereafter hardens, a strong, resilient seal is created between the two pieces. Substrates 40, 70 are conventional substrates used to fabricate CMOS electronic devices. Such substrates usually comprise silicon, although it will be recognized by those skilled in the art that the substrates may, for example, comprise GaAs, Ge or other semiconductor materials, or insulating materials such as quartz, alumina, or sapphire. For ease of description hereinbelow but without intending to limit the invention, it will be assumed that the substrates are silicon substrates.

The firewall 30 is fabricated around the MEMS device 25, and may be fabricated on either of the substrates 40, 70. The height of the firewall 30 can be precisely

controlled to thereby control the spacing between the two substrates. For some MEMS devices, the spacing may be an integral part of the MEMS device function, while in others it has to be simply large enough to accommodate the MEMS devices in the cavity 20. A sealing material is employed atop the firewall 30 to produce a hermetic seal 80 for the cavity 20. The sealing material is preferably a thin film metal material and is placed on at least a portion of the top 50 of firewall 30 to seal the cavity 20 when the second substrate 70 is flip-chip bonded to first substrate 40. During the flip-chip bonding process, the welding materials on both sides of the substrates are heated and pressed together, resulting in a tight hermetic seal between the flip-chip bonded substrates 40, 70. After the flip-chip bonding process, cavity 20 is bounded and formed by the firewall 30 and substrates 40, 70 and encloses a small space around the MEMS device 25. This leaves the MEMS device 25 intact and protected from subsequent packaging processes performed outside cavity 20, which might involve fluid treatment that have deleterious effects on the MEMS device 25.

The hermetic firewalls of the present invention can be fabricated using the same process that is employed for fabricating MEMS devices. In an example of MEMS devices fabricated using silicon surface micromachining technology, the firewalls may be made up of alternating stacks of polycrystalline silicon and silicon dioxide, encapsulated by polycrystalline silicon. Another alternative is to use a material that is deposited or spin-coated and patterned on a substrate using a lithography technique. Some examples include silicon nitride, polyimide and metal. In all cases, the material comprising the firewall 30 must have the desired chemical and mechanical strength to create a hermetic seal between the substrates and the firewall and to protect the MEMS device 25. Using such techniques, the height of the walls can be defined precisely.

In a preferred embodiment depicted in Figure 2, a hermetic seal 80 between the firewalls on first and second substrates can be formed by evaporating a soft metal such as gold, silver, or their alloys onto the top of firewall 30, and pressing down on the metal surface in a heated environment. The heated environment may be created

during the flip-chip bonding process of the first substrate to the second substrate itself, or by an independent heating or soldering process known to those skilled in the art. However, creating such a seal 80 usually does not provide enough mechanical strength to hold the substrates together and to provide mechanical integrity to the package 10. A stronger mechanical seal may be achieved using stronger solder, which is used in conventional flip-chip bonded packaging techniques. When it is desired to use additional solder to provide a stronger mechanical support, a plurality of solder bumps 90 can be bonded to the first substrate 40 which will provide mechanical support and integrity to the package, when the second substrate (not shown in Figure 2) is flip-chip bonded to the first substrate. Alternately, the solder bumps 90 may be bonded to the second substrate which is simply a matter of design choice.

Of critical importance in the fabrication of packages for MEMS devices in accordance with the present invention is that the electrical connection to the MEMS device 25 with the rest of the circuit must traverse firewall 30 without breaching the hermatic seal enclosing the cavity 20. In a preferred embodiment, electrical leads 100 connecting the MEMS device 25 to the rest of the circuit are inserted through firewall 30 during the MEMS fabrication process. In this case, for example, the leads can be made up of heavily doped conductive polycrystalline silicon, encapsulated by silicon dioxide layers to achieve electrical isolation. In another preferred embodiment, the electrical leads 100 can be placed underneath the firewall. Alternatively, leads 100 may be secured to the second substrate 70 that contains CMOS circuitry, for example, thereby alleviating the need to breach or otherwise corrupt the firewall 30 by requiring the leads 100 to physically traverse therethrough. In this case, vertical electrical connection between the MEMS device 25 on substrate 40 and the electrical leads on substrate 70 has to be fabricated. Such connection can easily be achieved by means of solder bumps or metallizing independent spacers 120 (Figure 3).

In the embodiment of Figure 2, the firewall 30 comprises stacks of poly-silicon and silicon dioxide layers. The firewall 30 itself also serves as a spacer for

cavity 20 to control the gap between the two substrates 40 and 70 so that cavity 20 has a height defined by the height of firewall 30. Mechanical strength is provided by independent solder bumps 90 placed outside the firewall 30. The solder bumps 90 may be placed at any convenient location on either or both of substrates 40, 70. The electrical leads 100 preferably comprise poly-silicon surrounded by silicon dioxide layers, encapsulated by another layer of poly-silicon.

Figure 3 depicts yet another preferred embodiment of the package 10 of the present invention having a hermetic firewall 30. A metal film as described above is evaporated on top 50 of the firewall structure and will form the hermetic seal 80 for the cavity 20. The solder material is deposited on top 50 of firewall 30 to produce a solder seal 110 for cavity 20. When the solder seal 110 is made, it provides both the hermeticity and mechanical strength necessary for the flip-chip bonding process to produce a sturdy, strong hermetic package. Independent spacers 120 may also be provided to accurately define the required gap or spacing between the substrates. Spacers 120 may be fabricated on either or both of substrates 40, 70 and may be placed at arbitrary locations thereon.

The process of solder bump or ring-shaped solder seal is schematically shown in Figures 4a-4c. In all preferred embodiments utilizing solder bump or ring-shaped solder seal bonding, the height of the spacers 120 are intentionally made higher than the solder bumps. For the solder bump preparation, one can deposit solder 75 onto a larger footprint than metal pad, over a dielectric layer 85 that the solder does not wet (Figure 4a). Upon heating, the surface tension will increase the solder bump 90 height and decrease its footprint (Figure 4b). This mechanism enables the solder bumps 90 to make contact to the mating metal pad 95 on the other substrate. Upon cooling, the solder shrinks and actively pulls the two substrates together (Figure 4c). This process guarantees an intimate connection between the spacers, and precise separation between the two substrates.

One disadvantage of the embodiment of Figure 3 is that if any flux material (either in the gas phase or the liquid phase) is necessary for soldering, the MEMS

device 25 will be exposed to this environment. This might not be detrimental to MEMS device 25 if the proper flux is used, but will limit the ability to provide a controlled environment for the MEMS device.

Figure 5 depicts still another preferred embodiment of the package 110 containing a hermetic firewall of the present invention. In this embodiment, a double-walled firewall structure is fabricated on either substrate 40, 70. The inner wall 130 is similar to that of Figure 1 wherein metal layers 80 are eposited on the top 50 of firewall 30, and provide the appropriate spacing for cavity 20. An outer wall 140 is similar to the firewall 30 of Figure 3 wherein a layer of solder material 110 is deposited on the top 50 of firewall 30. The mechanical strength for the resulting package is provided by the outer wall 140. In this embodiment, the inner wall 130 is bonded to either substrate 40, 70 with a "tack" bond between two metal layers 80 that is created by applying pressure between the two substrates at a low temperature as compared to the melting temperature of the solder of seal 110. When this process is accomplished in a controlled environment, the space encapsulated by the inner wall 130 maintains this environment and is sealed off. After the low-temperature tack bonding is accomplished, it is possible to simply heat up the substrate 40 or 70 to a temperature sufficient to melt the solder to thereby form the solder bond on outer wall 140. The double-walled firewall of Figure 4 thus advantageously protects MEMS device 25 from the deleterious effects of the soldering process.

The environment within the cavity defined by the firewall can be controlled by performing the flip-chip bonding process under the desired environment. Such desired environment may include, for example, controlled pressure, controlled humidity, and controlled gas chemistries. The cavity 20 created by this flip-chip bonding process protects the MEMS devices, so that the flip-chip bonded substrates can now be further packaged using conventional packaging techniques that might otherwise be detrimental to the MEMS devices.

While there have been shown and described certain fundamental novel features of the invention as applied to preferred embodiments thereof, it will be understood

that various omissions and substitutions and changes in the methods and apparatus described herein, and in their operation, may be made by those skilled in the art without departing from the spirit and scope of the invention. It is expressly intended that all combinations of those elements and/or method steps which perform substantially the same function in substantially the same way to achieve the same result are within the scope of the invention. Substitution of elements from one described embodiment to another are also fully intended and contemplated. It is the intention, therefore, to be limited only as indicated by the scope of the claims appended hereto.

Thus, while there have shown and described and pointed out fundamental novel features of the invention as applied to a preferred embodiment thereof, it will be understood that various omissions and substitutions and changes in the form and details of the devices illustrated, and in their operation, may be made by those skilled in the art without departing from the spirit of the invention. For example, it is expressly intended that all combinations of those elements and/or method steps which perform substantially the same function in substantially the same way to achieve the same results are within the scope of the invention. Moreover, it should be recognized that structures and/or elements and/or method steps shown and/or described in connection with any disclosed form or embodiment of the invention may be incorporated in any other disclosed or described or suggested form or embodiment as a general matter of design choice. It is the intention, therefore, to be limited only as indicated by the scope of the claims appended hereto.

4. Brief Description of Drawings

Written above.

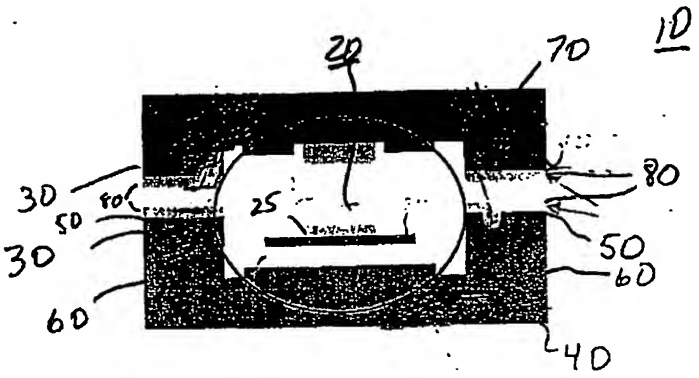


FIG. 1

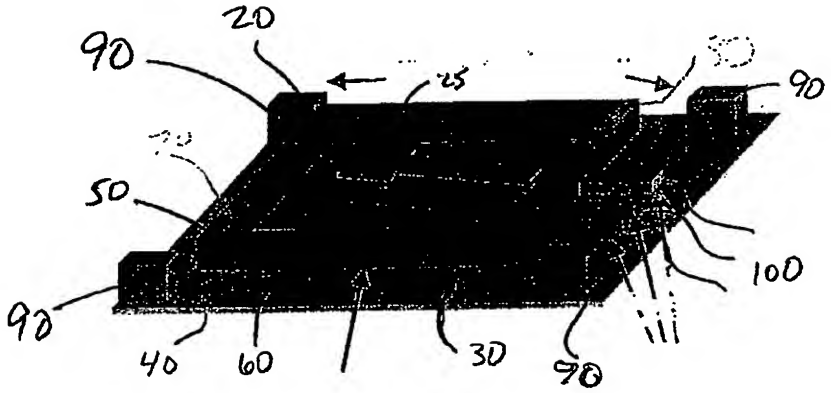


FIG. 2

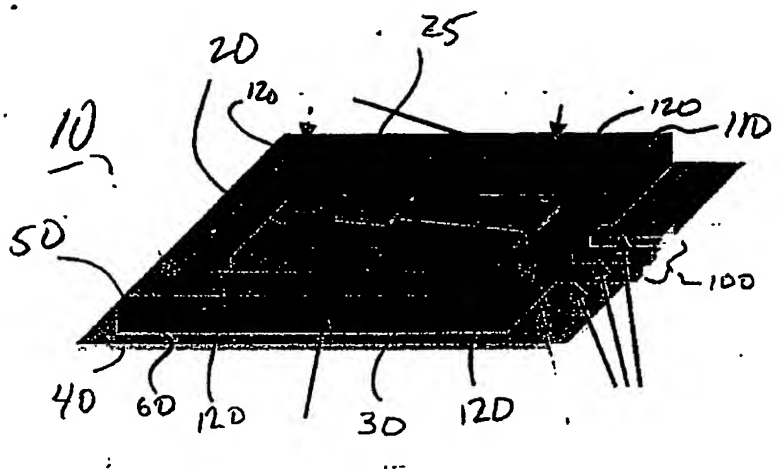
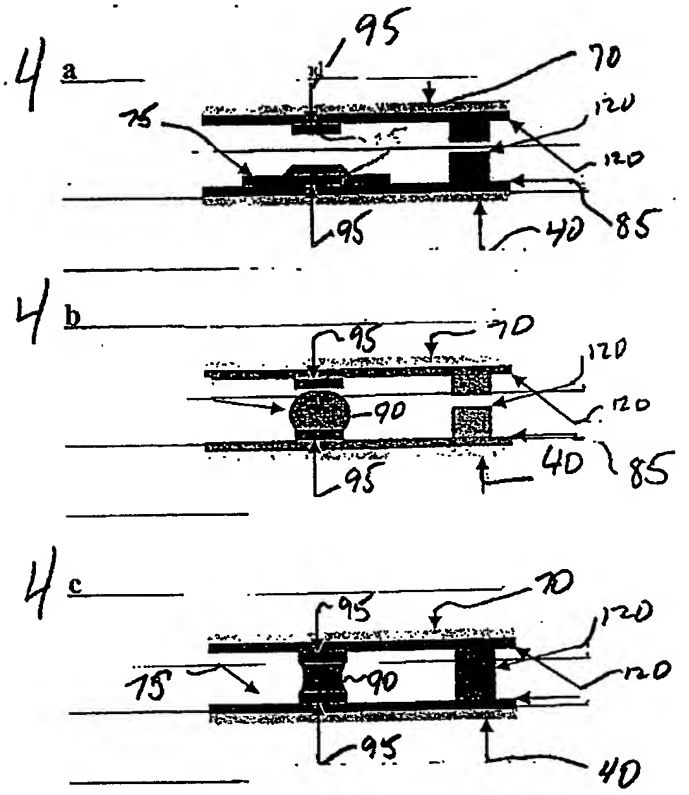


FIG. 3


4 a
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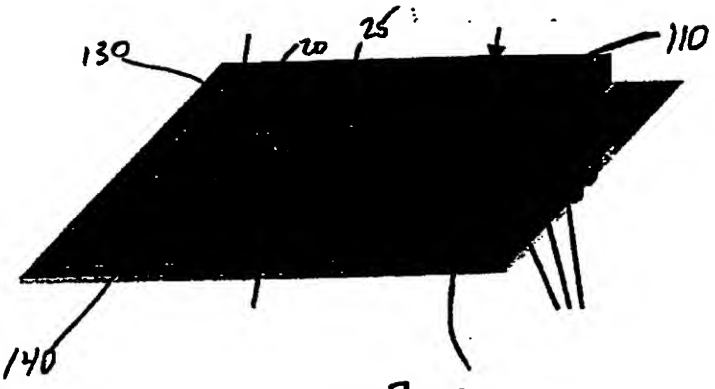
130
20
25
110
140
50

FIG. 5

1 Abstract

A package for hermetically sealing a micro-electromechanical systems (MEMS) device in a hybrid circuit comprise a firewall formed on a substrate for the MEMS device and which has a height defining a cavity of the package in which the MEMS device will be sealed. A second substrate spaced from the first substrate hermetically seals the cavity when the second substrate is flip-chip bonded to the first substrate and soldered to the first substrate with a thin film metal material placed on at least a top portion of the firewall. The resulting firewall MEMS device package can be further packaged using conventional CMOS packaging techniques. By hermetically sealing the cavity, the enclosed MEMS device is protected from deleterious conditions found in the environment of conventional CMOS packaging techniques which is often detrimental to MEMS device function.

2 Representative Drawing

Figure 1

Micromachining and Microfabrication '95, SPIE, Oct. 95.

Material and processing issues for the monolithic integrati n of microelectronics with surface-micromachined p lysilicon sensors and actuators

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ABSTRACT

The monolithic integration of micromechanical devices with their controlling electronics offers potential increases in performance as well as decreased cost for these devices. Analog Devices has demonstrated the commercial viability of this integration by interleaving the micromechanical fabrication steps of an accelerometer with the microelectronic fabrication steps of its controlling electronics. Sandia's Microelectronics Development Laboratory has integrated the micromechanical and microelectronic processing sequences in a segregated fashion. In this CMOS-first, micromechanics-last approach, conventional aluminum metallization is replaced by tungsten metallization to allow the CMOS to withstand subsequent high-temperature processing during the micromechanical fabrication. This approach is a refinement of an approach originally developed at U.C. Berkeley.

Specifically, the issues of yield, repeatability, and uniformity of the tungsten/CMOS approach are addressed. Also, material issues related to the development of high-temperature diffusion barriers, adhesion layers, and low-stress films are discussed. Processing and material issues associated with alternative approaches to this integration such as micromechanics-first, CMOS-last or the interleaved process are also discussed.

Keywords: micromechanics, CMOS, integration, tungsten, smart sensors

1. INTRODUCTION

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of microelectromechanical structures (MEMS) with driving, control, and signal-processing electronics. This integration promises to improve the performance of micromechanical devices as well as the cost of manufacturing, packaging, and instrumenting these devices by combining the micromechanical devices with an electronic subsystem in the same manufacturing and packaging process. For example, Analog Devices has developed and marketed an accelerometer[1] which illustrates the viability and commercial potential of this integration. They accomplished this task by interleaving, combining, and customizing their manufacturing processes which produce the micromechanical devices with the processes that produce the electronics. Researchers at Berkeley[2] have developed a modular integrated approach in which the aluminum metallization of CMOS is replaced with tungsten to enable the CMOS to withstand subsequent micromechanical processing.

2. INTEGRATION STRATEGIES

As presented in a recent review of integrated polysilicon microsystems[3], there are three basic approaches to monolithically integrating surface micromachined polysilicon devices with their controlling electronics: microelectronics-first, interleaved, and micromechanics-first. Each of these strategies must overcome the limitations of the processing requirements of both the microelectronic and micromechanical devices. Polysilicon micromechanical devices often have large vertical topologies (typically 4 to 10 microns in height) and require long, high-temperature anneals for stress relaxation (such as 3 hours at 1100°C). Microelectronic devices use precision photolithographic techniques that require planar substrates. They also have thermal processing budgets limited by dopant diffusion and metallization.

The microelectronics-first approach overcomes planarity restraint imposed by the photolithographic processes by building the microelectronics before the non-planar micromechanical devices. The limitation on thermal budget of the microelectronic devices remains a problem. Alth ugh the dopant diffusion problem is mitigated by changing the fabrication technology, the aluminum metallization used in conventional microelectronic technologies melts at the temperatures needed for polysilicon anneals. To overcome the temperature limitation of the aluminum metallization, researchers at Berkeley have prototyped an all-tungsten CMOS process. After having completed this process, the micromechanical devices are fabricated. A cross-sectional diagram of a modified version of the Berkeley process is shown in Figure 1. Unfortunately, the temperature of the polysilicon anneal is limited by the lack of a robust diffusion barrier to prevent formation of tungsten silicide during this anneal and by high stress of the tungsten film stack.

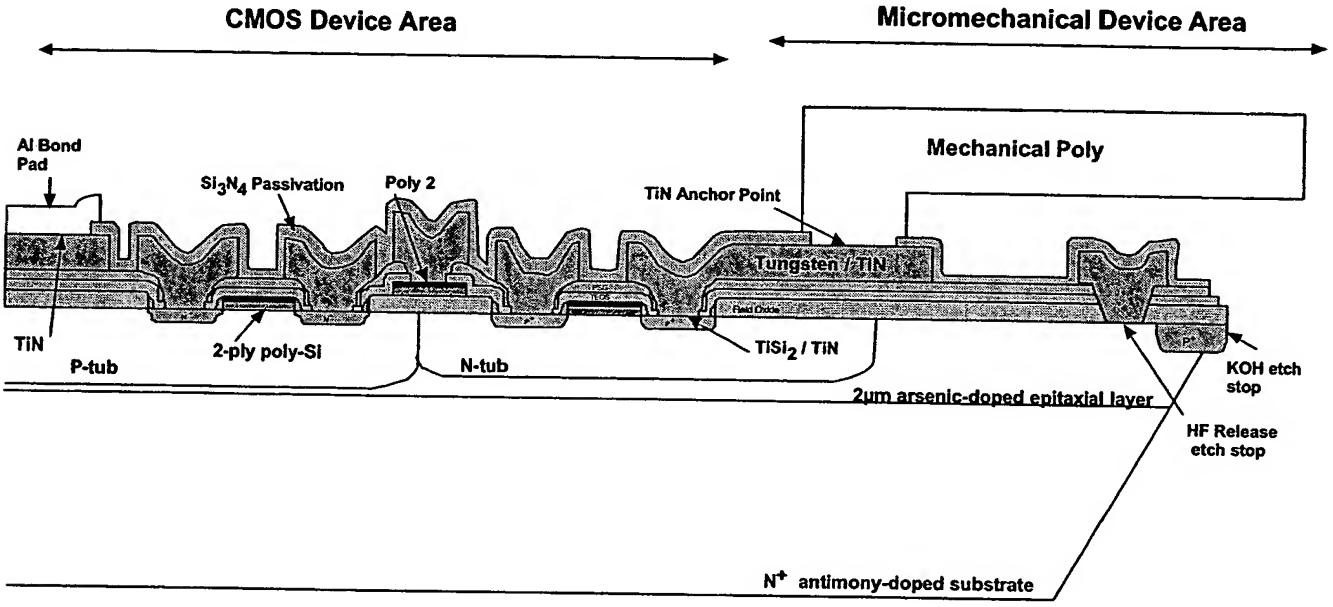

Figure 1. A cros-sectional view of the CMOS-first approach to micromechanical integration where tungsten metallization replaces the conventional aluminum metallization.

The interleaved approach may be the most economical for large-scale manufacturing since it optimizes and combines the manufacturing processes of both the micromechanical devices and the microelectronic devices. This optimized manufacturing mix imposes limits on both the microelectronic device performance and the micromechanical device performance. It also requires extensive changes to the overall manufacturing flow in order to accommodate changes in just the microelectronic devices or the micromechanical devices. This limits the usefulness of this approach for rapid prototyping of different technologies or development work.

Finally, a third approach to integration may be pursued. This micromechanics-first approach fabricates, anneals, and planarizes the micromechanical devices before the microelectronic devices are fabricated. Since the micromechanical devices are both annealed and planarized before the microelectronic device fabrication steps are reached, the topology and thermal processing limitations of the microelectronic devices are overcome. Figure 2 illustrates a micromechanics-first approach to integration that will be reported elsewhere.[4] In this technology, micromechanical devices are fabricated in trenches etched in silicon wafers. These trenches are then refilled with oxide, planarized by chemical-mechanical polishing, annealed, and sealed. These wafers then form the starting material for a conventional microelectronic fabrication process. This approach may also have advantages in packaging of finished devices.

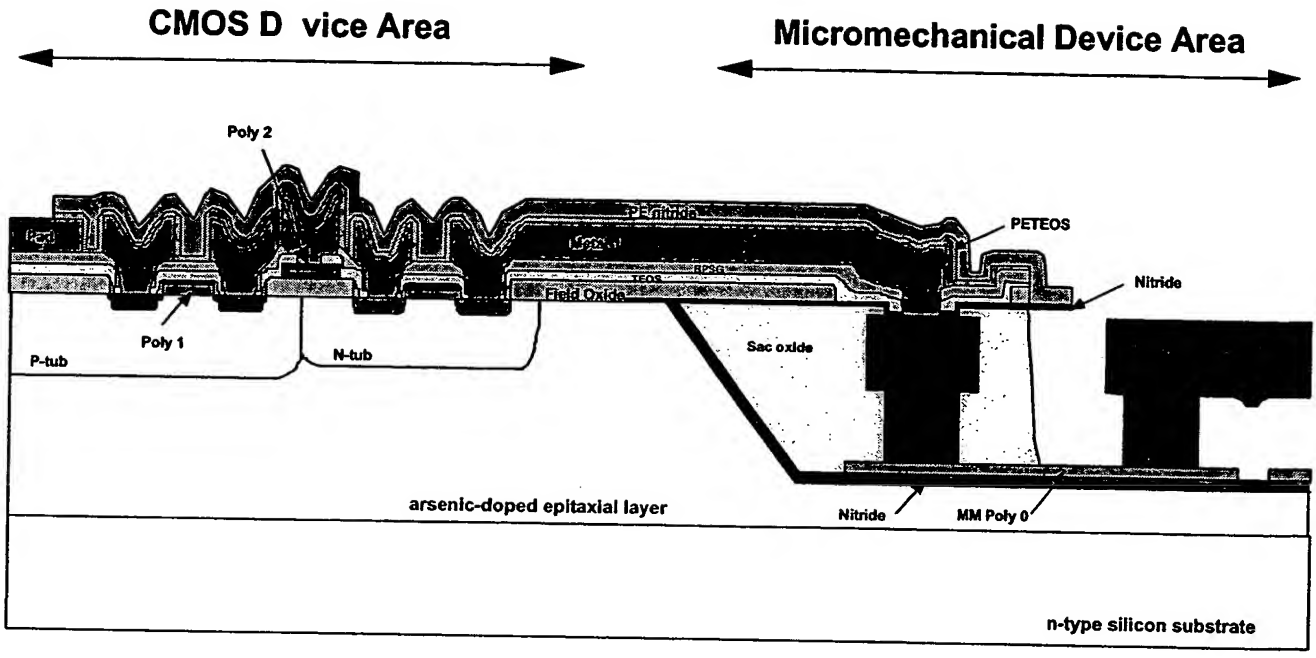

Figure 2. A cross-sectional view of the micromechanics-first approach to integration. Here, the micromechanical devices are built in a trench. This trench is then refilled with oxide, planarized, and sealed to form the starting wafer for CMOS processing.

3. CMOS-FIRST INTEGRATION RESULTS

A standard 2-micron, twin-tub CMOS process was modified to accomadate an all-tungsten metallization process. In order to separate the tungsten from the underlying silicon at the contacts an adhesion layer/diffusion barrier stack of 15 nm of selective TiSi followed 50 nm of TiN was used. The low-stress tungsten metallization was deposited by chemical vapor deposition to a thickness of 1 micron. Where tungsten metallization was deposited over the field oxide, only the TiN layer was used. Since it is difficult to attach Al or Au bond wires to tungsten, bond pads were formed by using the mechanical polysilicon deposited on top of a 50 nm TiN diffusion barrier and the 1 micron of tungsten. Difficulties were encountered during processing of wafers due to the compressive stress of the tungsten films, the surface roughness of low-stress tungsten, and sporadic failure of the TiN diffusion barrier during the micromechanical polysilicon anneal.

Figures 3 through 6 illustrate the threshold variation of n-channel and p-channel devices across a wafer both before and after the polysilicon anneal. These figures show functioning devices in both cases. No degradation of transistor performance was noted due to the micromechanical processing. Figures 7 and 8 show the contact resistance between the tungsten and the source/drain of n-type devices for a 2 micron by 2 micron contact. A small increase in contact resistance is seen after the anneal, but the average resistance is still less than 10 ohms. The non-uniformity of the post-anneal wafermap is probably due to poor temperature uniformity within the rapid thermal anneal system.

Figures 9 and 10 demonstrate a severe degradation in contact resistance between tungsten and p-type silicon. Here, the contact resistance has increased from 25 ohms to 125 ohms. This increase in contact resistance degrades the performance of the p-channel devices and may be due to out-diffusion of boron from the p+ source/drain implants in silicon.

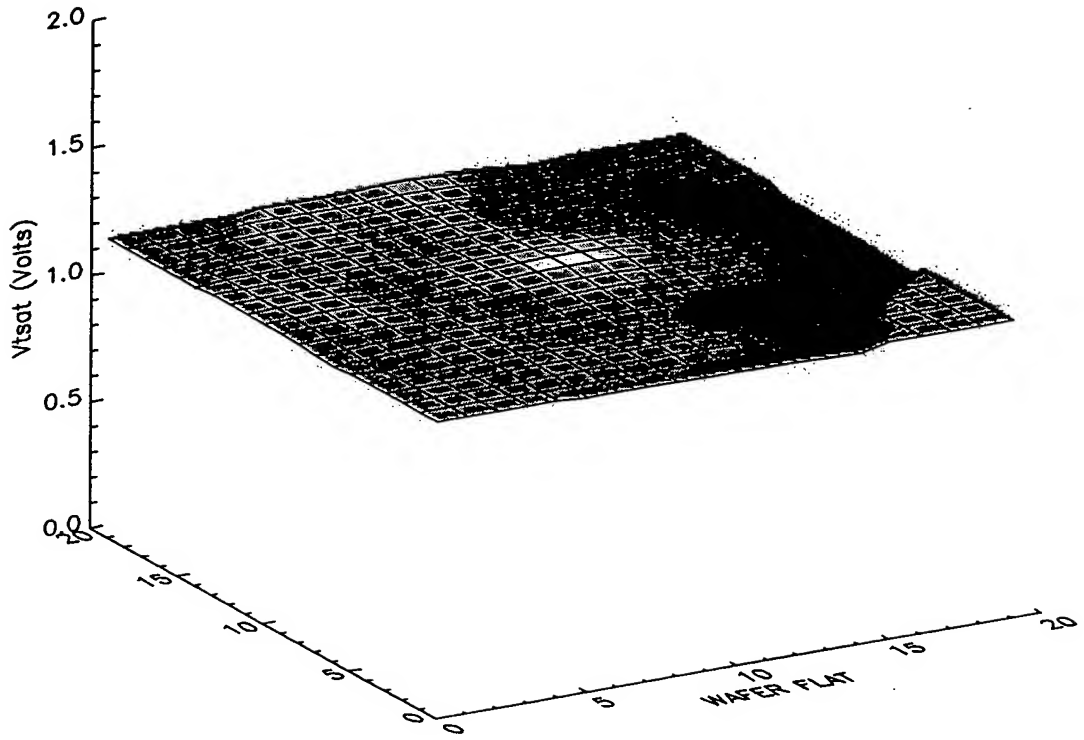

Figure 3. Threshold voltage wafer map for n-channel devices before the micromechanical anneal.

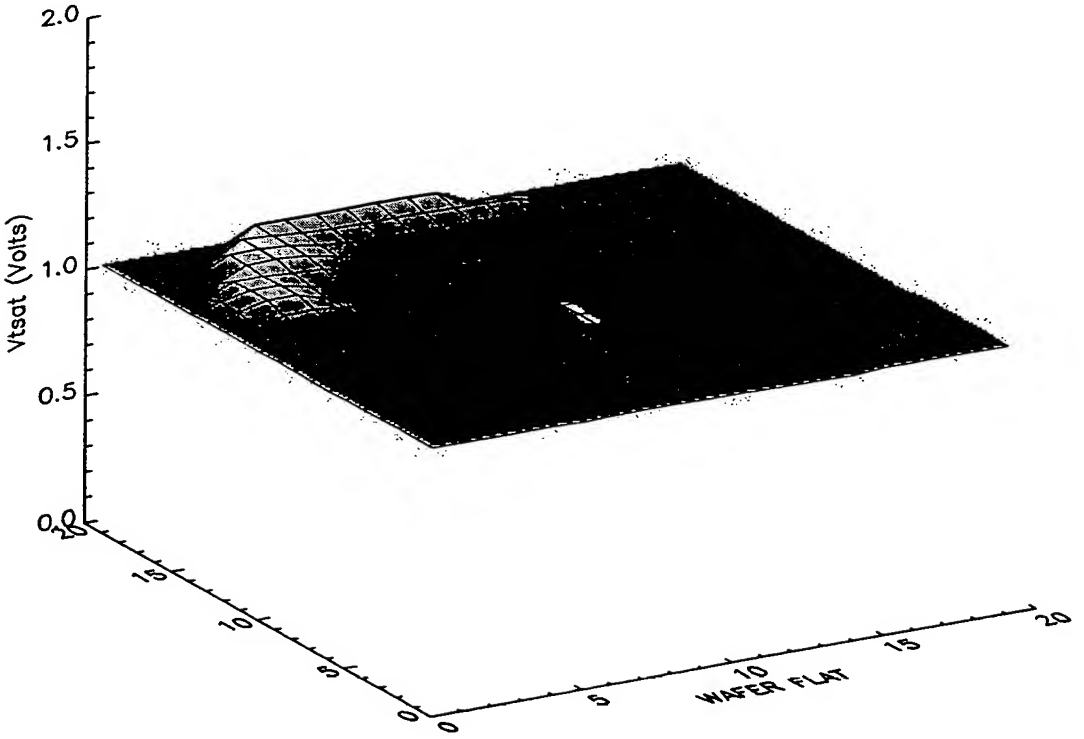

Figure 4. Threshold voltage wafer map for n-channel devices after the micromechanical anneal.

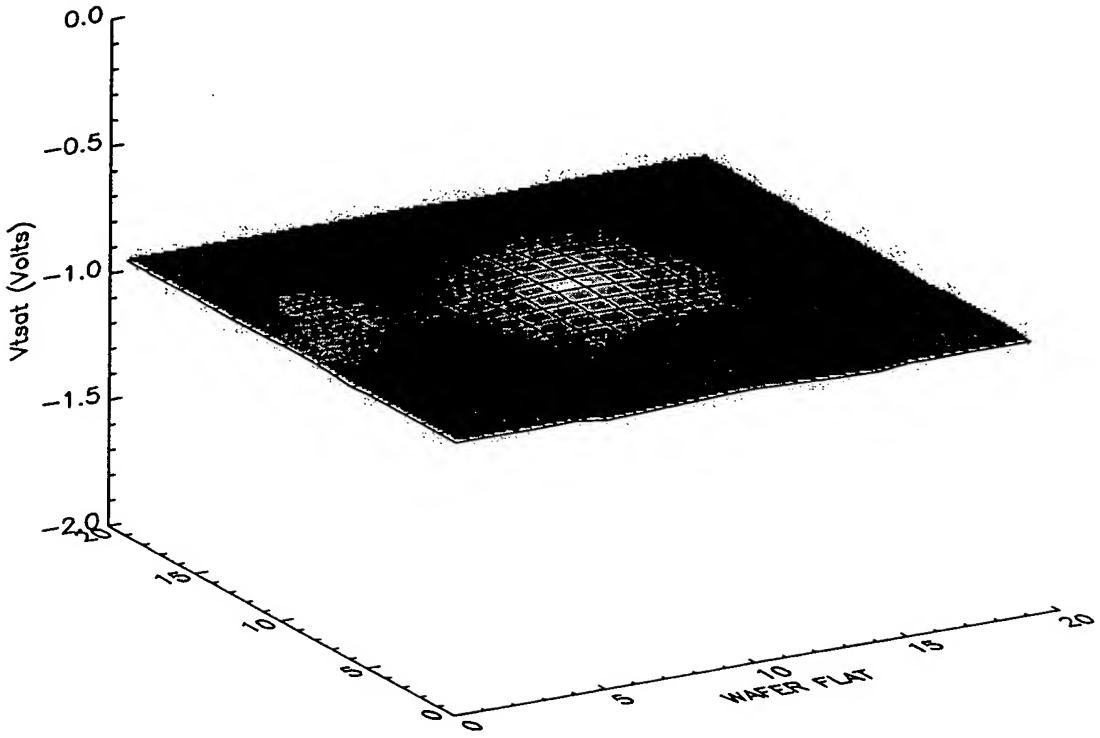

Figure 5. Threshold voltage wafer map for p-channel devices before the micromechanical anneal.

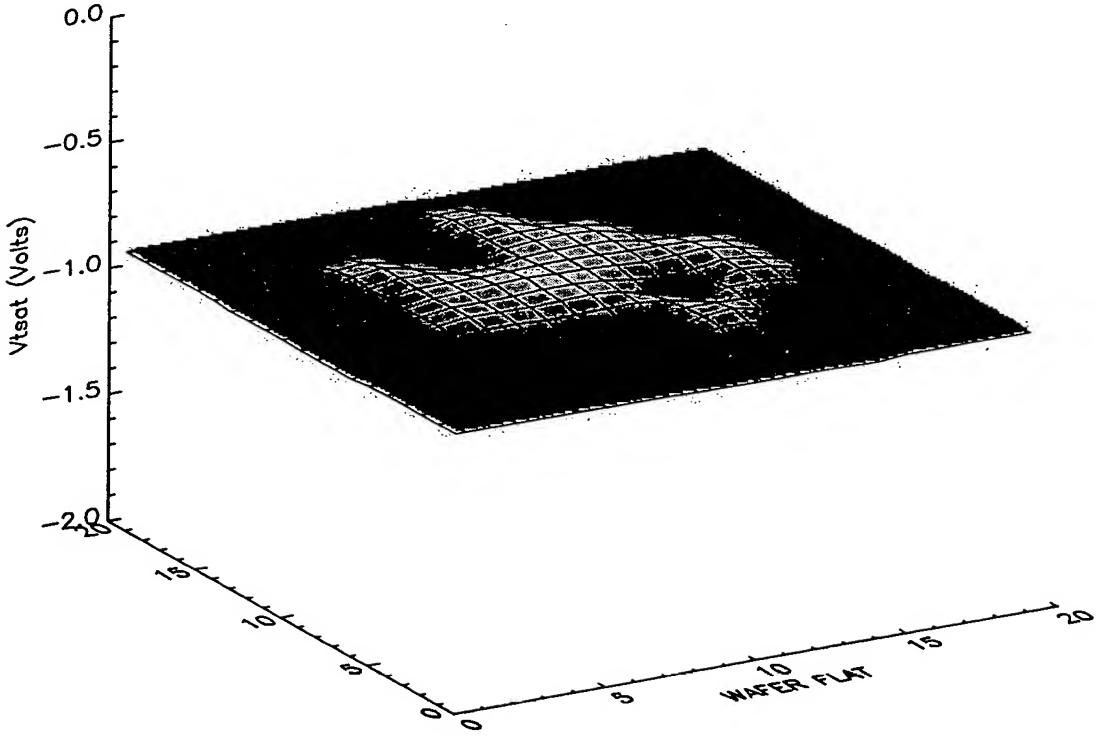

Figure 6. Threshold voltage wafer map for p-channel devices after the micromechanical anneal.

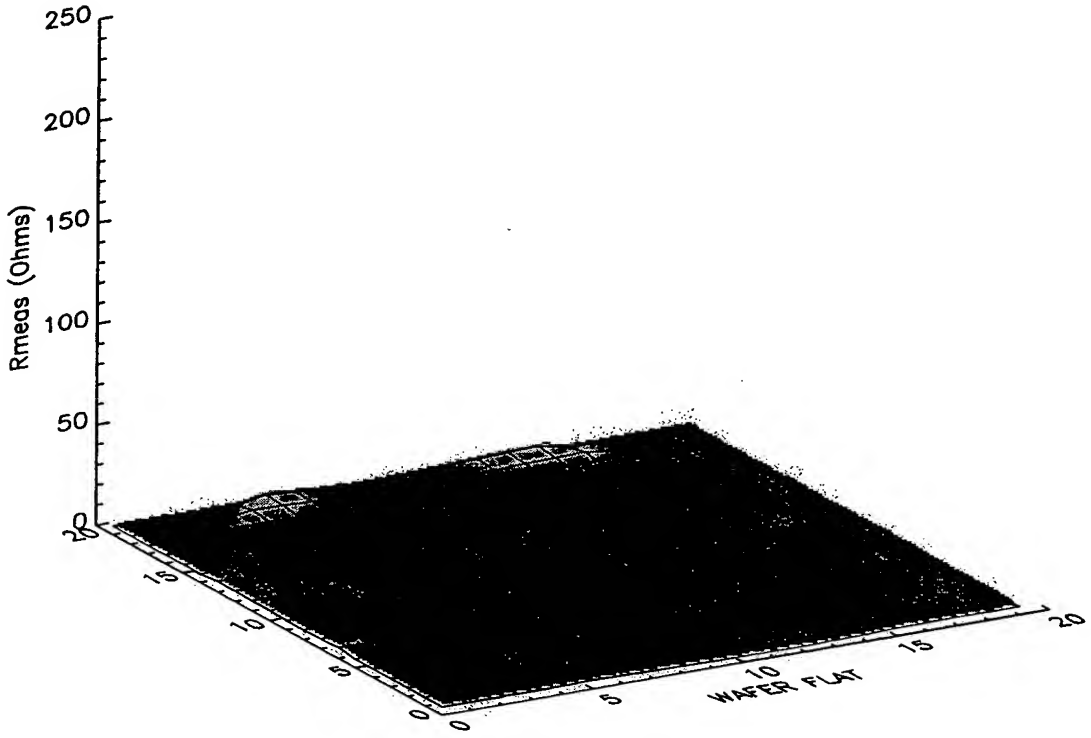

Figure 7. Wafermap of contact resistance between tungsten and n-type silicon before the micromechanical anneal.

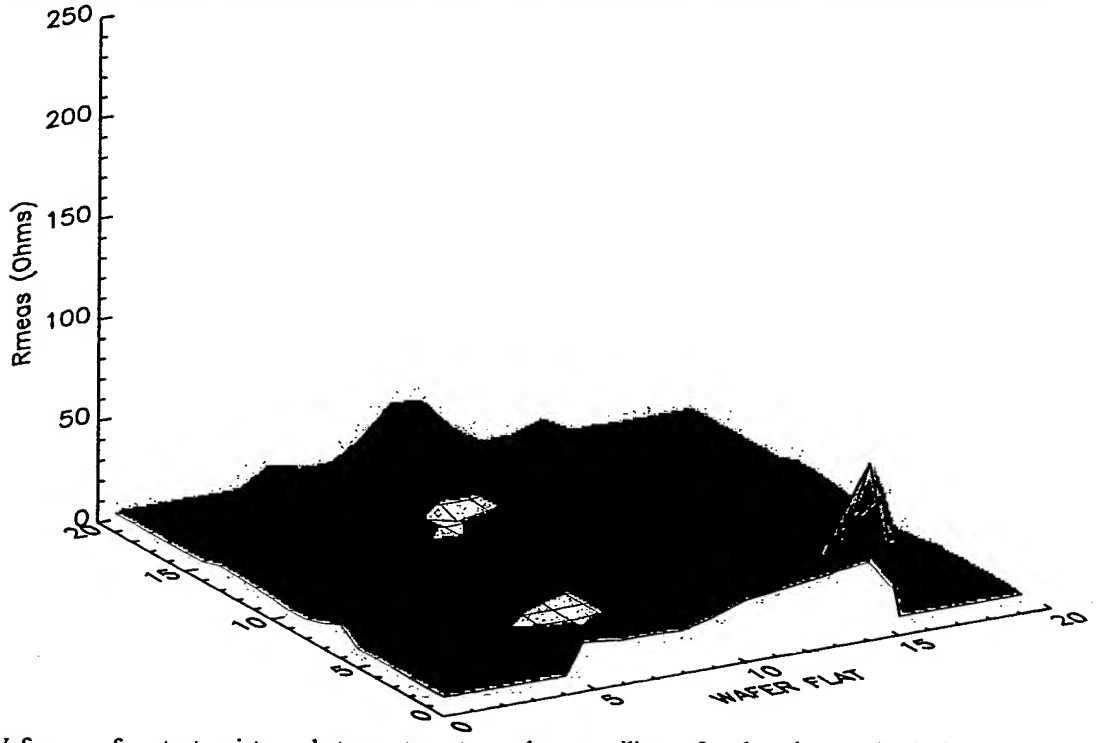

Figure 8. Wafermap of contact resistance between tungsten and n-type silicon after the micromechanical anneal

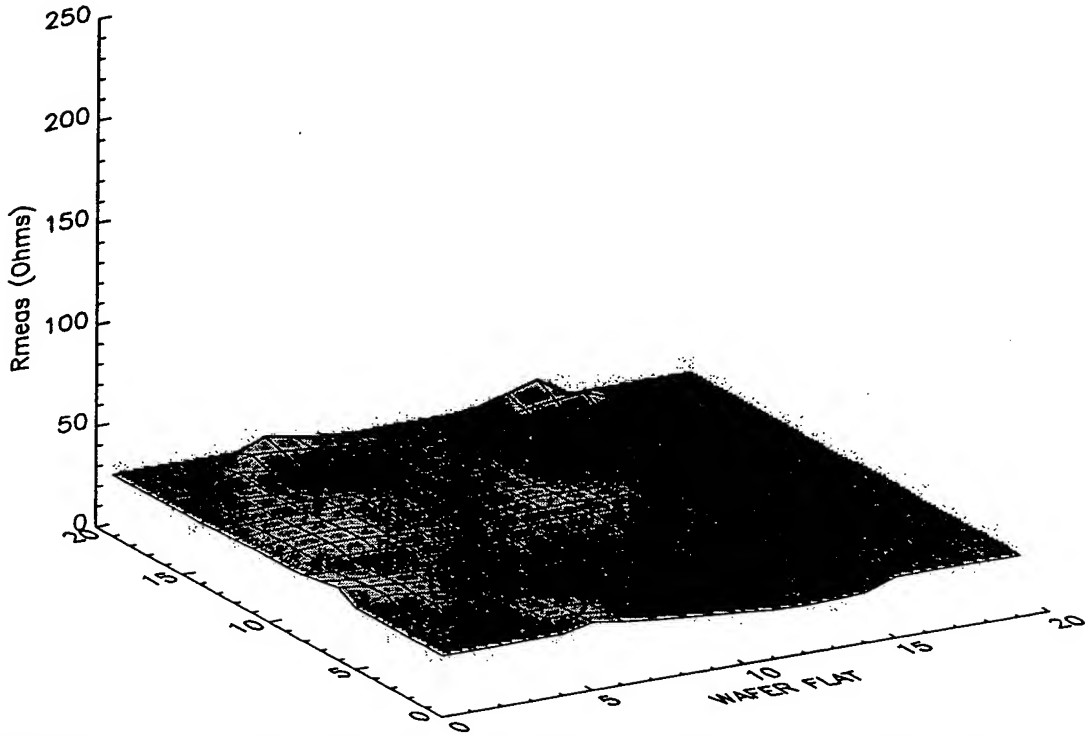

Figure 9. Wafermap of contact resistance between tungsten and p-type silicon before the micromechanical anneal

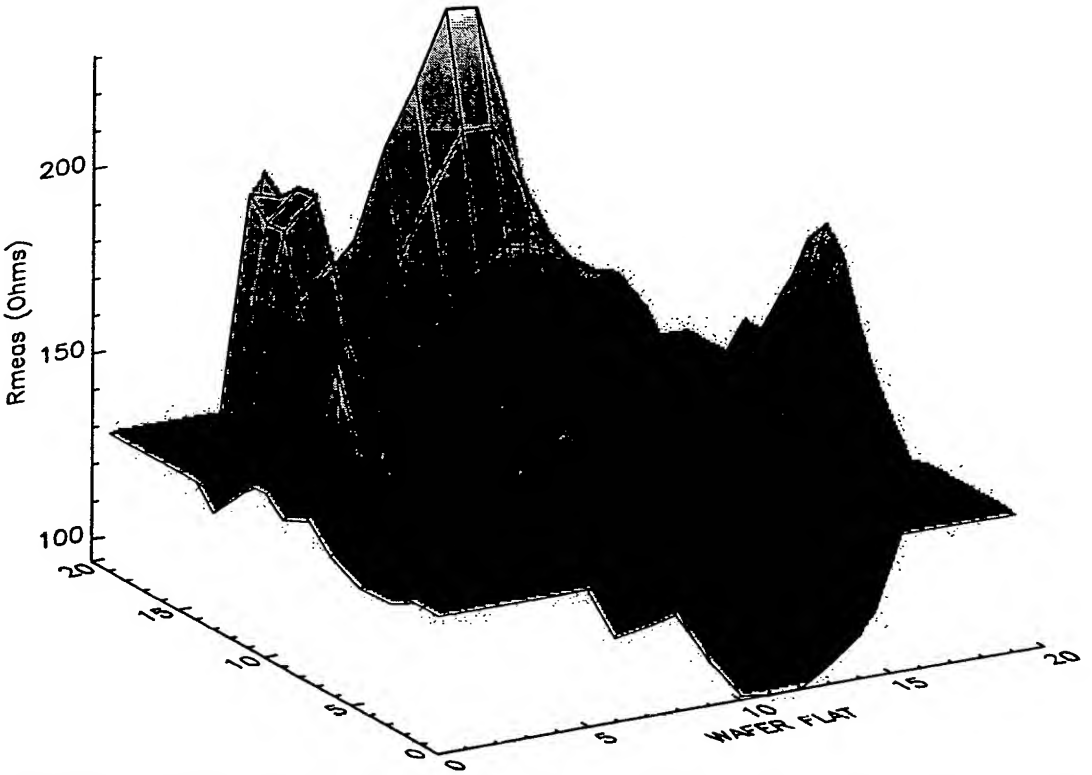

Figure 10. Wafermap of contact resistance between tungsten and p-type silicon after the micromechanical anneal. Note the change of scale.

The compressive stress of the bondpad stack caused delamination, or lifting, of the bondpads. Thin interconnect lines did not exhibit this lifting, but the 100 micron by 100 micron bondpads showed significant delamination. Figure 11 illustrates this phenomena. The delamination occurs between the field oxide and the silicon substrate. Figure 12 shows a cross-section of the delaminated bondpad in more detail. Starting from the bottom, the materials seen in this stack are TEOS-based field oxide, TiN, tungsten, porous WTiSi (formed by the failure of the upper TiN diffusion barrier), WSi, and micromechanical polysilicon.

In lowering the stress of the tungsten metallization by varying the deposition conditions, the surface roughness of the film was increased significantly. This prevented the use of projection steppers for photolithographically patterning the low-stress tungsten. A manually-aligned contact aligner was used instead.

Despite these processing difficulties, the devices fabricated were functional as long as their size was relatively small. A larger device, an accelerometer with on-chip preamplifiers is shown in Figure 13. The CMOS on this chip was fully-functional, but the temperature limitations imposed by the lack of a robust diffusion barrier caused the polysilicon to curl. For large polysilicon devices this curl prevented the micromechanical devices from being fully-functional. Devices under 200 microns in size did not see significant curling.

Because of the problems encountered in attempting to bring this technology to a manufacturing facility, we have decided to try other approaches besides the all-tungsten, CMOS-first integration approach.

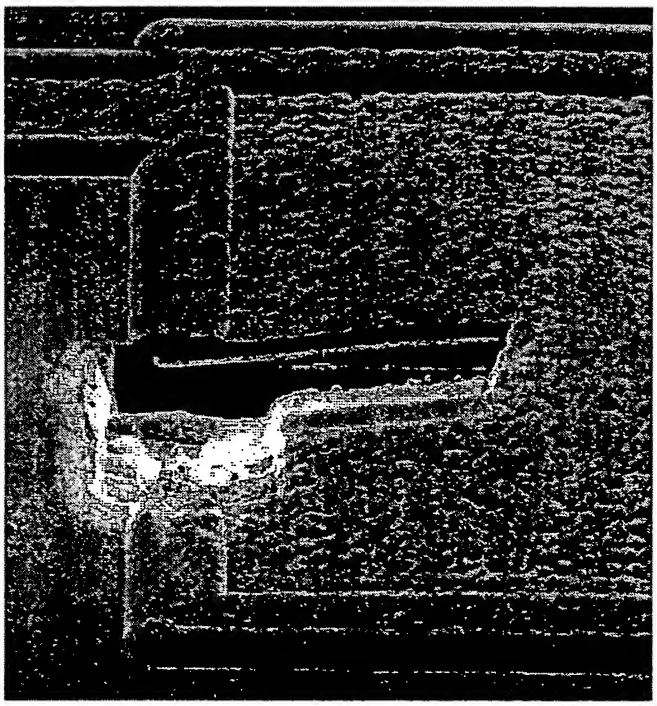

Figure 11. Focused ion beam cross-section of tungsten bondpad showing delamination of bondpad stack at the center of the contact due to compressive stress of bondpad stack.

Figure 12. Close-up view of the delaminated bondpad shown in Figure 11.

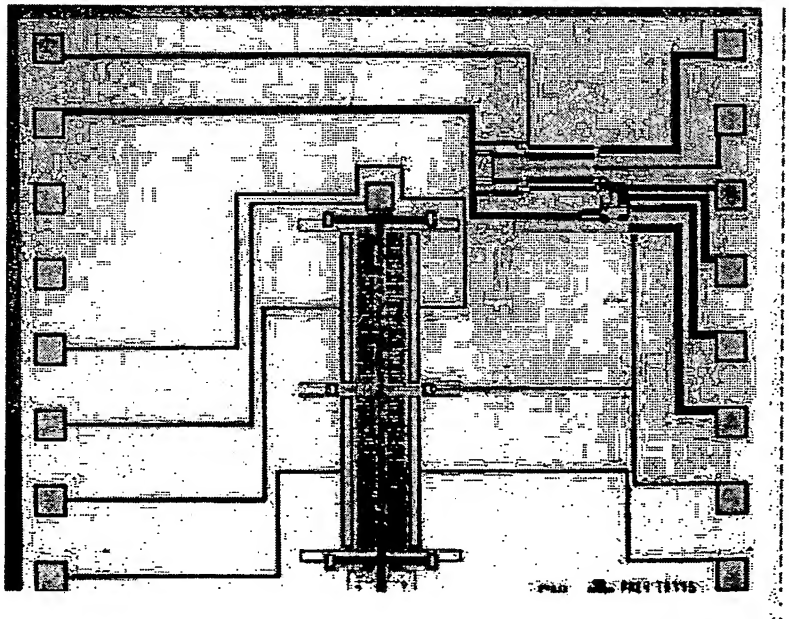

Figure 13. A surface-micromachined polysilicon accelerometer with integrated control electronics fabricated using the all-tungsten, CMOS-first approach to integration.

4. SUMMARY

Micromechanical structures require long, high-temperature anneals to assure that stress in the structural materials of the micromechanical structures has completely relaxed. On the other hand, CMOS technology requires planarity of the substrate to achieve high-resolution in the photolithographic process. If the micromechanical processing is performed first, the substrate planarity is sacrificed. If the CMOS is built first, it (and its metallization) must withstand the high-temperature anneals of the micromechanical processing. This second alternative was chosen by researchers at Berkeley and has been further developed as presented here. In this approach, the standard aluminum metal used in CMOS was replaced with tungsten. Since tungsten is a refractory metal, it withstands the high-temperature processing, but a number of issues remain unsolved concerning with adhesion of the tungsten layer and the unwanted formation of tungsten silicides. Despite these issues, devices integrated with functioning control electronics have been fabricated.

A unique micromechanics-first approach is also being developed. In this approach, micromechanical devices are fabricated in a trench etched on the surface of the wafer. After these devices are complete, the trench is refilled with oxide, planarized using chemical-mechanical polishing, and sealed with a nitride membrane. The wafer with the embedded micromechanical devices is then processed using conventional CMOS processing. Additional steps are added at the end of the CMOS process in order to expose and release the embedded micromechanical devices.

5. ACKNOWLEDGMENTS

This work, performed at Sandia National Laboratories, was supported by the U.S. Department of Energy under contract DE-AC04-94AL85000. The process development engineers, operators, and technicians of the Microelectronics Development Laboratory should also be acknowledged for their contributions to the process development, fabrication, and testing of these devices.

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